ISSN: 2277-9655
Scientific Journal Impact Factor: 3.449
(ISRA), Impact Factor: 2.114

IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

Design & Implementation of 8x8 Multiplier Unit using MT-CMOS Technique

Heena Naaz*, MD. Muqtar Ahmed, Panjala Kavitha
*Jyothishmati College of Engineering & Technology, Karimnagar, India
St.Marys College of Engineering And Technology, Hyderabad, India
Kakatiya Institute of Technology And Science, Warangal, India

Abstracts

This paper deals with various multipliers implemented using CMOS logic style and their comparative analysis on the basis of power and PDP (Power delay product). A variety of multipliers have been reported in the literature but power dissipation and area used by these multiplier circuits are relatively large. This paper proposed a high performance and power efficient 8x8 multiplier design based on Vedic mathematics using CMOS logic style. Power consumption plays an imperative role specifically in the field of VLSI today, every designer be it an analog circuit or a digital circuit designer is concerned about the amount of power his or her circuit is going to consume in the end. The use of Vedas not only abates the carry propagation taking place from lsb to msb but also produces the partial product and there sums in the same step. Vedic mathematics based multipliers thus causes least delay and consume least power than any other type of multipliers in the literature. The proposed MTCMOS implementation of Vedic multiplier is up to 24.55% power efficient and about 98% speedy as compared to the conventional CMOS implementation of Vedic multiplier

Keywords: 8x8 Miltiplier, MT-CMOS.

Introduction

The core of this paper consist of the introduction of a novel and high performance design of an 8x8 Multiplier using ancient Indian mathematics called Vedas. We have presented three different designs of the 8x8 Vedic multiplier using the CMOS technology, PTL and finally concoct the Vedic Multiplier using the Multi-Threshold Voltage CMOS (MTCMOS) and proved that the MTCMOS implementation of Vedic Multiplier is the best among all the implementations.

The use of Vedas not only abates the carry propagation taking place from lsb to msb but also produces the partial product and there sums in the same step. Vedic mathematics based multipliers thus causes least delay and consume least power than any other type of multipliers in the literature. The functionality of all the three designs and there PDP and total power consumptions at two different frequencies and three different voltages were calculated on tanner EDA 13.0v.

The demand for multipliers is continuously increasing as the fields like Communication, Signal Processing and fields involving high speed processors continue to snowball. One of the major operations involved in the above fields is multiplication and invention of high speed multipliers with advanced functionalities and high accuracy has been a grave matter of concern for past quite a lot of time.

Multipliers are inevitably used in almost every field of technology specifically electronics and communication, including Digital Signal Processing (DSP) and Image Processing (IP). They are widely used in the hardware implementation of Discrete Fourier Transform (DFT), Discrete Cosine Transform (DCT), and Discrete Sine Transform (DST) and there are different manifolds of multipliers that are used in Telecommunication and broadband communication industries. Gargantuan number of adders and other logic gates are required to carry out addition of partial products formed during the process of multiplication.

The essence of Vedic mathematics is the fact that it reduces the otherwise ponderous calculations in conventional mathematics that slows down the calculation process considerably. Vedic mathematics is commonly based on 16 Sutras (or aphorisms) dealing with different types of mathematics like arithmetic, algebra, geometry etc. Most generic form of multipliers used in the industries and other practices involves array multiplier, algebraic transformational multiplier, booths multiplier, bit serial multiplier. Multiplication requires carry propagation from the least significant bit (LSB) to the most significant bit (MSB) during the addition of binary partial products thus the latency incurred is during the addition and subtraction of the binary products formed after multiplication.

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Vedic mathematics is a part of four Vedas (books of wisdom). It is part of Sthapatya- Veda, which is an upa-veda (supplement) of Atharva Veda. It encompasses the explanation of numerous modern mathematical terms that includes arithmetic, geometry, trigonometry, quadratic equations, factorization and even calculus. This is a very enticing field and presents some efficient algorithms which can be applied to numerous branches of engineering such as computing, image processing and digital signal processing. The word "Vedic"was coined from the word "Veda" which means the repertoire of all knowledge. Vedic mathematics is commonly based on 16 Sutras (or aphorisms) dealing with different types of mathematics like arithmetic, algebra, geometry etc.
This paper proposed a high performance and power efficient 8x8 multiplier design based on Vedic mathematics using CMOS logic style. CMOS technology when scaled helps in the attainment of reduced supply and threshold voltages. When the threshold voltages are lowered the sub threshold current begins to wax precipitously. The highly recommended circuit technique for the leakage current reduction is the Multi- Threshold Voltage CMOS (MTCMOS).

Multiplication method using VEDAS

Vedic mathematical system consisting of sixteen basic Sutras (i.e. formulas).these 16 sutras have their own individual significance. The Urdhva-Tiryagbyham means vertically and crosswise, Ekadhikina Purvena means next is one more than previous, Nikhilam Navatashcaramam Dashatah means all are subtracted from 9 and the last is subtracted from 10, Paraavartya Yojayet means transpose and then adjust, Shunyam Saamyasamuccaye means when the sum is same then that sum is zero, (anurupye) Shunyamanyat means if one is in ratio then other is zero, Puranapuranabyham means completion and non-completion, Chalana-Kalanabyham means differences and similarities, Yaavadunam means whatever the amount of its deficiency, Vyashtisamanstih means part and whole, Shesanyankena Charamena means last digit's remainder, Sopaantyadvayamantyam means the ultimate and twice of the penultimate, Ekanyunena Purvena means by one less than previous one, Gunitasamuchyah means the sum's product is equal to the product's sum, Gunakasamuchyah means the sum's factor is equal to the factor's sum.

Usage of these Sutras have been majorly done for the multiplication of two numbers in the decimal format. In this work, we extrapolated the same ideas to the binary number to make the proposed algorithm compatible with the digital hardware. From the above defined sixteen sutras we are using one sutra that is Urdhva-Tiryagbyham to implement the Vedic multiplier. The Proposed Vedic Multiplier can be used to reduce Delay. As compared to Array Multiplier, Proposed Vedic Multiplier is efficient in terms of delay and speed.

With the help of these sutras,we have designed a 8x8 multiplier, which successfully saves power consumption, enhancing the usage of supply power.

Urdhav-Tiryagbyhamv method:

This sutra(formula) is perfect for all types multiplication. It means "vertically and crosswise" as shown in Fig. 1.

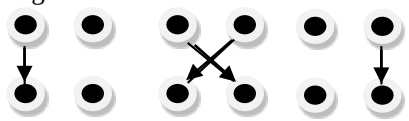


Fig. 1. Urdhav method.

consider an example of multiplication of two numbers A1=11 and B2=19. The steps are followed according to the steps shown in Fig. 2.Initially, we need to multiply the unit digit of the two numbers vertically that is multiplication of 1and 2. Step 2 consists of crosswise multiplication of unit digit of second number to tense digit of first number and unit digit of first to tens digit of second number and then addition of the results of two crosswise multiplications is done, that is addition of 9(product of 1 and 9) and 1(product of 1 and 1) giving carry as 1. In step 3 vertical multiplication of the digits at tens place is carried out giving 1 (multiplication of 1 and 1). In step 4 the result of step 3 is added with the carry generated in the step 2 giving 2(addition of 1 and 1). The result is produced by writing the result of step 4, the digit obtained by eliminating the carry in the result of step 2 and the result of step 1 as 209.

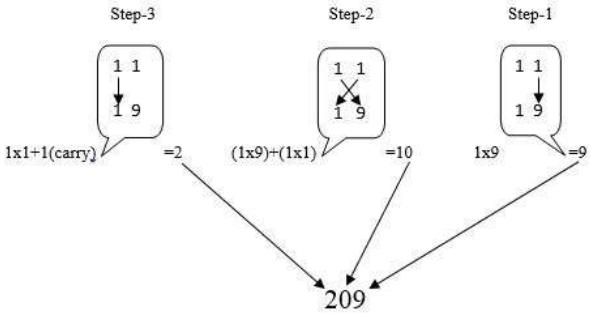


Fig. 2. Multiplying two numbers using Urdhav method.

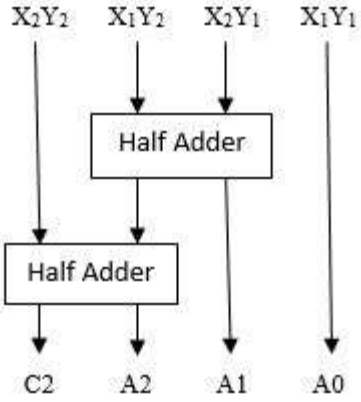
VEDIC multiplier using mtcmos technique

The implementation of 2x2-bit Vedic multiplier is structured by using four AND gates and two HA as shown in Fig. 3. The first Half Adder is used to add outputs of AND gates having input a1b0 & a0b1 and second Half Adder are used to add carry generated from

ISSN: 2277-9655
Scientific Journal Impact Factor: 3.449
(ISRA), Impact Factor: 2.114

1st Half Adder and output of AND gate having input a1b1.

Here, both Partial product generation and addition is performed concurrently. Therefore, it is adaptive to parallel processing. The 2x2 bit Vedic multiplier has inputs as X_2 X_1 and Y_2 Y_1. To understand the concept, the Block diagram of 2x2 bit Vedic multiplier is shown in below Fig. 3. To get final product two Half Adders are required. As compared to Array Multiplier, Proposed Vedic Multiplier is efficient in terms of delay and speed. The Proposed Vedic Multiplier can be used to reduce Delay.



Leakage current plays a pivotal role in modern high performance integrated circuits (ICs) as more than 35% to 40% of the total active mode energy is associated with these currents. CMOS technology when scaled helps in the attainment of reduced supply and threshold voltages. When the threshold voltages are lowered the sub threshold current begins to wax precipitously. Additionally, it is the leakage current which is the prime source of energy consumption in an idle circuit. Integrating more transistors on-chip, causes the leakage current to dominate the high performance IC's total energy consumption. In various hand-held battery-operated gadgets like mobile phones, laptops etc. employs long standby periods thus reducing the leakage current is highly important to provide longevity to the battery.

The highly recommended circuit technique for the leakage current reduction is the Multi-Threshold Voltage CMOS (MTCMOS). In MTCMOS technology, efficient power management is obtained by allowing the circuit to operate in two modes: 1) Active Mode 2) Sleep Mode.

The circuit makes use of two different set of transistors – one being the High Vt transistors known as the "sleep" transistors and other being the Low Vt transistors which forms the logical circuit. The sleep transistors helps in the reduction of leakage current thus providing the high performance and the Low Vt transistors are used to boost the circuit's speed performance.

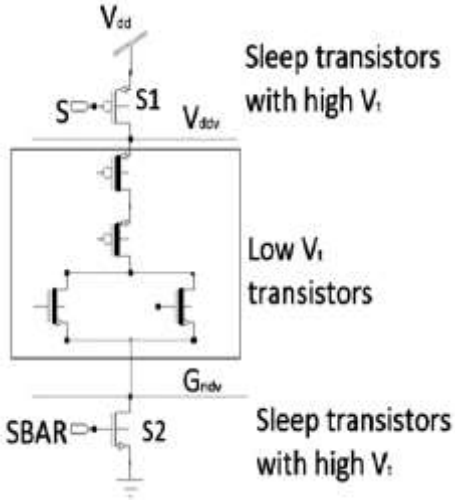


Fig. 4. Power Gating Technique using MTCMOS.

The circuit shown in fig.4 comprises of two sleep transistors S1 and S2 which possess the higher Vt . The logical circuit between S1 and S2 comprises of the Low Vt transistors is not connected directly to the real supply, Vdd and ground, Gnd but is connected to virtual supply and ground lines Vddv and Gndv. The sleep transistors are provided with complementary inputs S and SBAR.The circuit works in the active mode when, S=0 and SBAR=1 thus making both the sleep transistors S1 and S2 to remain ON and the virtual supply and ground lines Vddv and Gndv works as real supply lines and the logic circuit performs its operations normally at higher speed. But when S=1 and SBAR=0, the circuit works in the sleep mode making S1 and S2 sleep transistors to go in OFF state which results in the floating of virtual power supply lines and sleep transistors S1 and S2 suppresses the large leakage current present in the circuit. This reduces the power consumption as the leakage current has been lowered.

ISSN: 2277-9655
Scientific Journal Impact Factor: 3.449
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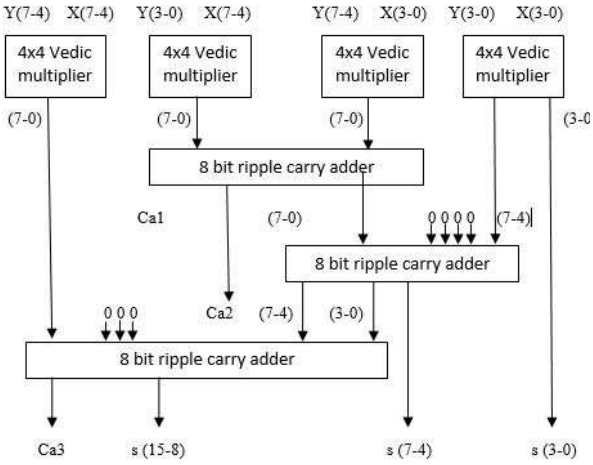

Fig.5 Block diagram of 8X8 bit Vedic multiplier.

The 8X8 bit Vedic multiplier shown in Fig. 5 can be implemented by using four 4X4 bit Vedic multiplier modules. Analysing 8X8 multiplications, inputs are X7-X0 and Y7-Y0 and the multiplication's 16 bits output will be s15-s0. In this , four 4X4 bit Vedic multipliers and three 8 bit RC Adders(having 2 input of 8 bits) are required. Inputs are given to the 4x4 bit Vedic multipliers and the output of multiplier is of 8 bits. Now, the input of the 1st RC Adder is the output of the 2nd and 3rd 4x4 bit multipliers which gives output of 8 bits (7-0) + one carry. The 2nd RC Adder will add the output of 1st RC Adder (7-0) and 4 bits (7-4) output of 1st 4x4 bit Vedic multiplier, other 4bit of are considered as 0.So output is of 8-bits(7-0) and one carry(carry is discarded). The 3rd RC Adder will add the output of 4th 4x4 bit multiplier(7-0) and 4 bits of output of 2nd RC Adder (7-4), other 4 bits are carry of 1st RC Adder and 0.Now , the output of 8x8 multiplier is s(3-0) output of 1st 4x4 bit multiplier(3-0), s(7-4) is output of 2nd RC Adder (3-0) and s(15-8) = 8 is output of the 3rd RC Adder(7-0).

Results and comparision

Power consumption and Power Delay Product (PDP) comparisons for 8x8 bit Vedic-CMOS, 8x8 bit Vedic-PTL and 8x8 bit MT-Vedic multipliers at different voltages and for 50MHz and 100 MHz frequencies is shown in below fig.6 and fig.7 respectively. Implementation of 8x8 bit Vedic multiplier using CMOS logic, PTL logic and using MTCMOS technique using the 90nm technology has been carried out on Tanner EDA tool.

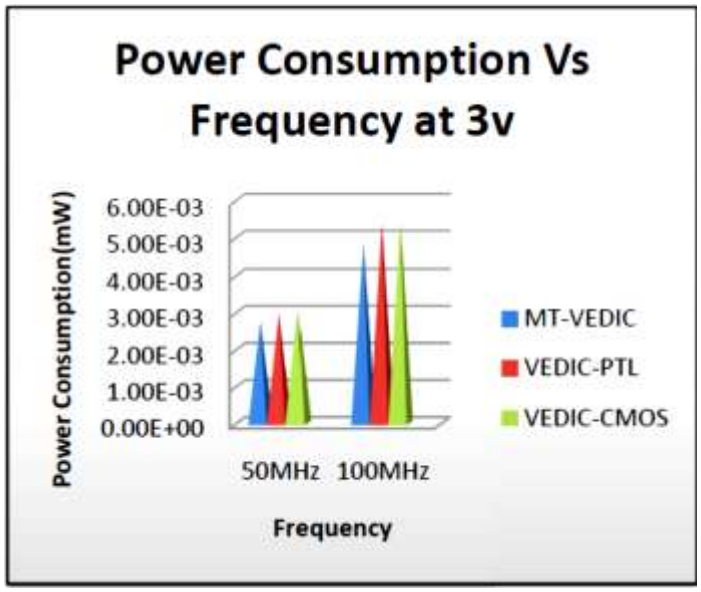

Fig. 6. Power Consumption Vs Frequency At 3v

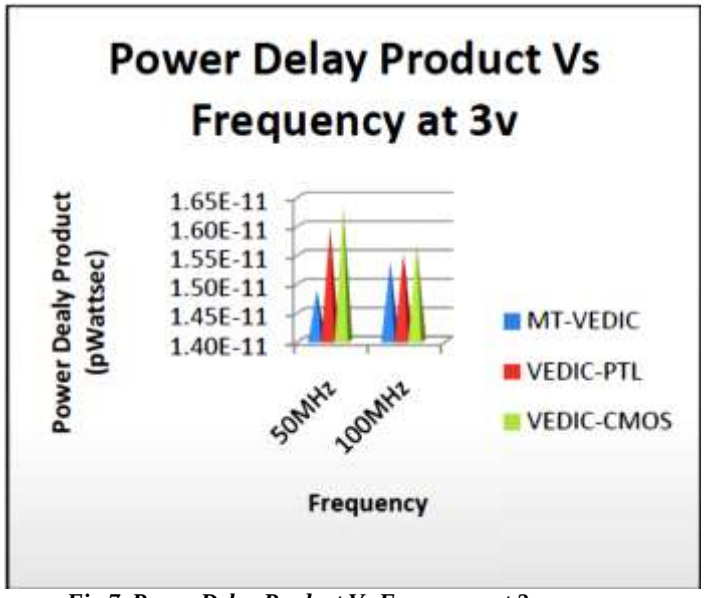

Fig.7. Power Delay Product Vs Frequency at 3v

At 1v for 50MHz there is a reduction of 11.37% in power consumption by Vedic-PTL as compared to Vedic-CMOS. But at same set of values MTVedic outperforms Vedic-PTL by providing a 14.86% power reduction. Similarly comparing there PDP's at 2v for 50MHz Vedic-PTL has 91.48% reduced PDP than Vedic-CMOS and MT-Vedic again outperforms Vedic-PTL by showing a 71.13% reduced PDP. The conclusion that we can draw from this is that MT-Vedic outshines both Vedic-PTL and CMOS in power consumption and PDP and shows 24.55% reduction in power consumption and 97.54% reduction in PDP compared to Vedic-CMOS.

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Conclusion

Power consumption and time delay play an important role in the vlsi design today.with the use of vedic multiplier we are able to achieve efficient power consumption and time accurate vlsi design with good accuracy .the vedic multiplier boosts up the time delay and performs the task at a high speed. The 90nm MTCMOS vedic multiplier is upto 25% power saving and also 98% faster compared with the other conventional multipliers.

References

1. Ramalatha, M.Dayalan, K D Dharani,ppriya, s deoborah, High Speed Energy Efficient ALU Design using Vedic Multiplication Techniques", International Conference Tools for Engineering Applications (ACTEA) IEEE, pp. 600-603,july 15-17, 2009.
2. Jagadguru Swami, Sri BharatiKrisna,tirthaji maharaja, vedic Mathematics or Sixteen Simple Mathematics formulae from the veda, Delhi (1965)", MotilalBanarsidas, Varanasi India, 1986.
3. P. K. Saha, A. Banerjee, and A. Dandapat,"High Speed Low Power Complex Multiplier Design Using Parallel Adders and Subtractors, "International Journal on Electronic and Electrical Engineering,(JEEE), Vol 07, no. II, pp. 38-46, Dec. 2009.
4. S. He, and M. Torkelson, "A pipelined bit-serial complex multiplier using distributed arithmetic," in proceedings IEEE International Symposium on Circuits and Systems, Seattle, W A, April 30- May03,1995,pp. 2313-2316.
5. P.Mehta and D. Gawali, "Conventional versus vedic mathematical method for Hardware implementation of a multiplier."In proceedings IEEE international conference on Advances in computing, control and Telecommunication Technologies.Trivandrum, kerala, Dec.28-29, 2009, pp.640-642.
6. C. S. Wallace, "A suggestion for a fast multiplier," IEE Trans Electronic Computer., vol. EC-13, pp.14-17, Dec.1964.
7. H. D. Tiwari, G. Gankhuyag, C. M.Kim, and Y.b.Cho,"Multiplier design based in ancient Indian Vedic Mathematics," in Proceeding IEEE International SoC Conference, Bussan, Nov 24-25,2008,pp.65-68.
8. Z. Huang, and M. D. Ercegovanc, "High-Performance Low Power Left- to-Right Array Multiplier Design," IEEE Transactions in computers, vol54,no.3,pp 272-283,March 2005.
9. T.Aoki ,K.Hoshi, and T. Higuchi, "Redundant complex arithmetic and its application to complex multiplier design ," in proceedings 29th IEEE International symposium on Multiplier -Valued-Logic, Freiburg, May 20-22,1999 , pp.200-207.